

APPARATUS FOR CIRCUIT WITH KEEPER

Field of the Invention

5 The invention related to a keeper circuit. In particular, the invention related to a keeper circuit for ensuring that the high-range and low-range outputs of a circuit utilizing voltage doubling techniques are actively driven.

Background

10 Voltage doubling is a technique that makes it possible to design electrical circuits that operate with high power supply voltages (e.g. 10V or above), while not allowing the Vgs, Vgd, or Vds of the individual transistors in the circuit to exceed a lower value, such as 5V. The voltage doubling technique is often implemented with cascode transistors. In general, voltage doubling techniques may be used to extend the operating range to
15 approximately 2X volts, where the underlying components can withstand X volts.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings, in which:

20 Figure 1 illustrates a schematic diagram of a circuit that includes a keeper switch;
Figure 2 shows a schematic diagram of an exemplary embodiment of the circuit of Figure 1;

Figure 3 illustrates a schematic diagram of an exemplary embodiment of an inverter circuit with a keeper switch;

25 Figure 4 shows a schematic diagram of another exemplary embodiment of an inverter circuit with a keeper switch;

Figure 5 illustrates a schematic diagram of an exemplary embodiment of a level translator circuit with a keeper switch;

30 Figure 6 shows a schematic diagram of another exemplary embodiment of a level translator circuit with a keeper switch; and

Figure 7 illustrates a schematic diagram of another exemplary embodiment of a level translator circuit with a keeper switch, arranged in accordance with aspects of the present invention.

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Detailed Description

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached 10 hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The 15 meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the 20 items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

25 Briefly stated, the invention is related to a circuit with a keeper switch that is configured to minimize capacitive coupling between the gate and drain of a transistor arranged in a cascode configuration. The keeper switch is coupled between the source and gate of the cascode transistor. The keeper switch is active if a voltage at the drain of the keeper switch circuit corresponds to a first logic level. If this event occurs, the source 30 and gate of the cascode transistor are coupled together.

Figure 1 illustrates a block diagram of a circuit (100) that includes a keeper switch circuit. Circuit 100 includes a first transistor (M0) and a second transistor (M1) configured in a cascode arrangement (104), and a keeper switch circuit (102). The second transistor (M1) has a gate that is coupled to a bias node (N12), a drain that is 5 coupled to a first output node (N1), and a source that is coupled to a second output node (N2). The keeper switch circuit (102) has three terminals that are respectively coupled to the gate of the second transistor (M1), the drain of second transistor (M1), and the source of the second transistor (M1). The second transistor (M1) is configured to receive a first cascode bias voltage (bias) at the bias node (N12). The first cascode bias voltage (signal 10 bias) is suitable as a cascode bias voltage.

The keeper switch circuit (102) is configured to influence a resistance between the second output node (N2) and the bias node (N12) in response to a control signal (e.g. signal bias). The keeper switch circuit (102) is configured to couple the second output node (N2) to the bias node (N12) if the control signal corresponds to a first logic level. 15 The keeper switch circuit (102) is further configured to isolate the second output node (N2) from the bias node (N12) if the control signal corresponds to a second logic level.

In Figure 2, circuit 200 is a particular implementation of circuit 100, where the keeper switch circuit (102) is implemented by a transistor (M8). Transistor M8 has a gate that is coupled to the first output node (N1), a source that is coupled to the second output 20 node (N2), and a drain that is coupled to the bias node (N12). Alternatively, the drain may be coupled to the second output node (N2), and the source may be coupled to the bias node (N12).

Figure 3 illustrates a schematic diagram of a circuit (300) that is an exemplary implementation of circuit 100. Circuit 300 is a high-voltage inverter that utilizes 25 voltage doubling techniques. Circuit 300 includes transistors M2-M3 and M6-M7, and keeper switch circuit 102. Keeper switch circuit 102 is implemented by transistor M8. Transistor M8 has a gate that is coupled to node N1, a source that is coupled to node N2, and a drain that is coupled to node N11.

Transistors M2 and M3 are each arranged to operate as a cascode transistor. 30 Transistor M2 is configured to receive a first bias signal V_{sp} at a gate of transistor M2 (node N11), and transistor M3 is configured to receive a second bias signal V_{sn} at a gate

of transistor M3 (node N13). Signal V_{sp} is a cascode bias voltage that is used to bias transistor M2, and signal V_{sn} is a cascode bias voltage that is used to bias transistor M3. The voltages associated with signals V_{sp} and V_{sn} are set by several factors including the power supply voltage, the maximum V_{gs} , V_{gd} , and V_{ds} of the process for relatively 5 long-term reliability, the threshold voltages of the transistors, the junction diode breakdowns of the transistors, and the input voltage swing. Signals V_{sp} and V_{sn} are selected such that the maximum V_{gs} , V_{gd} , and V_{ds} of the transistors for relatively long-term reliability are not exceeded.

Transistor M6 is configured to receive a high-range signal in_hr at the gate of 10 transistor M6, and transistor M7 is configured to receive a low-range signal in_lr at the gate of transistor M7. Signal in_lr is bounded between 0 volts and approximately $V_{dda}/2$, where V_{dda} is the voltage associated with the power supply. Signal in_hr is bounded between V_{dda} and approximately $V_{dda}/2$. Signal in_hr and signal in_lr each correspond to substantially the same logic level at approximately the same time. A high-range output signal (hr) is provided at the drain of transistor M6 (node N2). The logic 15 level associated with signal hr corresponds to the inverse of the logic level of signals in_lr and in_hr . Circuit 300 is also configured to provide a full-range output signal (fr) at the source of transistor M2 (node N1), and a low-range output signal (lr) at the source of transistor M3 (node N3). Signals fr and lr each correspond to the same logic level as signal hr, but are bounded over different ranges. Signal lr is bounded between 0 volts and 20 approximately $V_{dda}/2$, signal hr is bounded between approximately $V_{dda}/2$ and V_{dda} , and signal fr is bounded between 0 volts and V_{dda} .

Transistor M8 is configured to ensure that signal hr is actively driven regardless 25 of the voltage associated with signals in_hr and in_lr , even at initial power-on. Transistor M8 is arranged for preventing charge injection (i.e. capacitive coupling) that could otherwise be caused as a result of the gate-to-drain capacitance on transistor M6. If present, injected charge could cause a voltage at the gate of transistor M6 to move outside of the desired operating range for V_{gs} , V_{ds} , and V_{gd} of transistors M6. According to the example illustrated in Figure 3, transistor M2 is a p-type transistor, and transistor M8 is a 30 p-type transistor.

Figure 4 illustrates a schematic diagram of a circuit (400) that is another exemplary implementation of Figure 1. Circuit 400 is substantially similar to circuit 300 in some ways, albeit different in other ways. In circuit 400, keeper switch circuit 102 is implemented by transistor M9. Transistor M9 has a gate that is coupled to node N1, a drain that is coupled to node N13, and a source that is coupled to node N3.

5 Transistor M9 is configured to ensure that signal lr is actively driven independent of the voltage associated with signals in_hr and in_lr, including at the initial power-on state. Transistors M3 and M9 are n-type transistors.

Figure 5 illustrates a schematic diagram of a level-shifter circuit (500). Circuit 10 500 includes transistors M2-M5 and M11-M16, keeper circuit 102 (transistor M8) and another keeper circuit (transistor M10). Transistor M4 has a gate that is coupled to node N11, a drain that is coupled to a first complement output node N21, and a source that is coupled to a second complement output node N22. Transistor M10 has a gate that is coupled to node N21, a source that is coupled to node N22, and a drain that is coupled to node N11.

Transistor M8 is configured to operate in a substantially similar manner as described with regard to Figure 3, albeit different in some ways. Transistor M4 is arranged to operate as a cascode transistor in cooperation with transistor M12. Transistor M5 is configured to operate as a cascode transistor in cooperation with transistor M14. 20 Circuit 500 is configured to provide signals hr, fr, lr, hrb, frb, and lrb in response to a data input signal (din). Signal hrb is a complement of signal hr, signal frb is a complement of signal fr, and signal lrb is a complement of signal lr. As an example, transistors M2, M4, M8, and M10 are each p-type transistors. Transistor M8 is configured to ensure that signal hr is actively driven regardless of the voltage associated with signal din. 25 Transistor M10 is configured to ensure that signal hrb is actively driven regardless of the voltage associated with signal din.

Figure 6 illustrates a schematic diagram of a circuit (600) that is substantially similar to circuit 500, albeit different in some ways. In this embodiment, the keeper circuit 102 is implemented by transistor M9, and the other keeper circuit is implemented 30 by transistor M17. In this example, transistors M3, M5, M9, and M17 are n-type

transistors. Transistor M9 is configured to ensure that signal I_r is actively driven. Transistor M17 is configured to ensure that signal I_{rb} is actively driven.

Figure 7 illustrates a schematic diagram of a circuit (700) that is substantially similar to circuit 600, albeit different in some ways. In this embodiment, keeper circuit 5 102 is implemented by transistor M19, and the other keeper circuit is implemented by transistor M18. Keeper switch circuit 102 and the other keeper switch circuit are each coupled respectively to nodes N3, N13, and M23. Transistor M19 has a gate that is coupled to node N23, a source that is coupled to node N13, and a drain that is coupled to node N3. Transistor M18 has a gate that is coupled to node N3, a source that is coupled 10 to node N13, and a drain that is coupled to node N23.

In this example, keeper switch circuit 102 is configured to influence a resistance between nodes N3 and M13. Keeper switch circuit 102 is configured to receive a control signal (e.g. signal I_{rb} at node N23). Also, the keeper switch circuit 102 is further configured to couple node N3 to node N13 if the control signal corresponds to a first 15 logic level (e.g. low). Additionally, keeper switch circuit 102 is further configured to isolate node N3 from node N13 if the control signal corresponds to a second logic level (e.g. high). In this example, transistors M3 and M5 are n-type transistors, and transistor M18 and M19 are p-type transistors.

The above specification, examples and data provide a description of the 20 manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention also resides in the claims hereinafter appended.